

# BHARAT INSTITUTE OF ENGINEERING & TECHNOLOGY

**SIVARAM VIHAR, GHATAKESWAR HILLS  
MOHADA, BERHAMPUR (GM.)**



## STUDENT'S ATTENDANCE REGISTER

Time \ Day	9:05	9:55	10:45	11:35	12:25
Day	9:55	10:45	11:35	12:25	1:15
Mon			DEC		
Tue			DEC		
Wed	DEC Lab				
Thu				DEC Lab	
Fri			DEC		
Sat	DEC				

Year/ Session : 2023 (winter)

Semester from Date: 01/08/2023 To Date : 30/11/2023

Semester & Branch

3<sup>rd</sup> sem & E&TC

Subject with Code

Digital Electronics & Th-3

Name of the Faculty Member

P. Anjali Bisoi

No of Weeks:

No of Days per Week Class Allotted : 4

# B.I.E.T., COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
A U G U S T	1st	2/8/23	<p style="text-align: center;"><u>Unit-1</u></p> <p style="text-align: center;"><u>Basics OF Digital Electronics</u></p> <p>1.1 Number system - Binary, octal, Decimal, Hexadecimal, - conversion from one system to another system.</p> <p>1.2 Arithmetic operation Addition, Subtraction, Multiplication, division, 1's &amp; 2's complement of binarys &amp; subtraction using complements method.</p> <p>1.3 Digital codes &amp; its application &amp; distinguish between weighted &amp; non-weighted code, Binary codes, excess-3 &amp; gray codes.</p>
		4/8/23	
		5/8/23	
	2nd	7/8/23	
		8/8/23	
		11/8/23	

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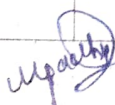
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 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD:

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 1/8/23

# B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
	3 <sup>rd</sup>	12/8/23 14/8/23	1.4 Logic Gates : AND, NOR, NAND, OR, Exclusive-OR, Exclusive-NOR - symbol, function, expression, truth-table, & timing diagram.
		16/8/23 19/8/23	1.5 Universal gates & its realization.
			1.6 Boolean algebra, Boolean expression, Demorgan's theorem
	4 <sup>th</sup>	21/8/23 25/8/23 26/8/23	1.7 Represent logic expression, SOP & POS forms.
			1.8 Karnaugh map (3 & 4 variable) & minimization of logical expressions, don't care condition

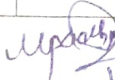
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# B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
S E P T E M B E R			Unit-2
			<u>Combinational Logic Circuits</u>
	5 <sup>th</sup>	28/8/23	2.1 Half adder, full adder, Half subtractor, full subtractor
	1 <sup>st</sup>	1/9/23	Serial & parallel binary adder.
		2/9/23	
	2 <sup>nd</sup>	4/9/23	2.2 Multiplexer (4:1), De-multiplexer (1:4), decoder, encoder, Digital comparator (3bit).
		5/9/23	
		8/9/23	
		9/9/23	
	3 <sup>rd</sup>	11/9/23	2.3 Seven segment decoder. (Definition, relevance, gate level of circuit logic circuit, truth table, applications of above)
		12/9/23	
		15/9/23	

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# B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
O C T O B E R			2.4 <u>Unit-3</u> <u>Sequential Logic Circuit</u>
	4 <sup>th</sup>	16/09/23 18/9/23	3.1 Principle of flip-flops operations, its types.
	5 <sup>th</sup>	22/9/23 23/9/23 25/9/23 ''	3.2. SR flip-flop using NAND, NOR, Latch (unclocked).
	2 <sup>nd</sup>	26/9/23 30/9/23 31/10/23	3.3 clocked SR, D, JK, T JK Master slave flip-flop logic circuit, truth-table and applications.
		5/10/23 7/10/23	3.4 Concept of Latching & how it can be avoided.

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th	Week	Class Day	Theory/Practical Topic
O C T O B E R	3 <sup>rd</sup>	9/10/23	<u>Unit-4</u> <u>Registers ; Memories &amp; PLD</u>  4.1 shift Registers - serial - in-serial out, serial - in - parallel out, parallel - in - serial - out, & parallel - in - parallel - out.
		10/10/23	
		13/10/23	
	4 <sup>th</sup>	16/10/23	4.2 Universal shift registers. Applications.
		17/10/23	4.3 Types of counters & Applications
	6 <sup>th</sup>	20/10/23	4.4 Binary counter, Asynchronous ripple counter, (up & down) decade counter, synchronous counter, ring counter.

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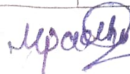
Month	Week	Class Day	Theory/Practical Topic
N O V E M B E R	1st	3/11/23 4/11/23	4.5 Concept of memories - RAM, ROM, Static RAM, Dynamic RAM, PS RAM.  4.6 Basic concept of PLD & applications.

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Month	Week	Class Day	Theory/Practical Topic
N O V E M B E R	2nd	6/11/23	<u>Unit-5</u> <u>A/D and D/A Converters</u>
		7/11/23	5.1 Necessity of A/D & D/A Converters.
		10/11/23	5.2 D/A Conversion using R-2R or weighted resistor methods.
		11/11/23	5.3 D/A Conversion using R-2R ladder (weighted resistors) n/w.s.
	13/11/23	5.4 A/D Conversion using Counter method.	
3rd	13/11/23	5.5 A/D Conversion using Successive approximate method.	

Signature of the Faculty:  17/8/2023

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Month	Week	Class Day	Theory/Practical Topic
N O V E M B E R	3rd	14/11/23	<u>Unit-6</u> <u>Logic Families</u> 6.1 Various logic families and categories according to the IC fabrication process.  6.2 Characteristics of digital ICs - propagation delay, fan-out, fan-in, power dissipation, Noise Margin, power supply requirement, and speed with reference to logic families.
		17/11/23	
	4th	18/11/23	
		20/11/23	
		21/11/23	
		24/11/23	

Signature of the Faculty: *Upadhyay* / 11/8/2023

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# B.I.E.T., COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
	5 <sup>th</sup>	25/11/23 28/11/23	6.3 Features, circuit oper <sup>n</sup> , and various applications of TTL (NAND), CMOS (NAND & NOR).

*Seep  
Mediyans*

*Upadhyay*  
Signature of the Faculty: 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD: *Pradyumn*  
1/8/23