BHARAT INSTITUTE OF ENGINEERING & TECHNOLOGY

SIVARAM VIHAR, GHATAKESWAR HILLS
MOHADA, BERHAMPUR (GM.)

STUDENT'S ATTENDANCE REGISTER

Time / Day	9:05 – 9:55	9:55 – 10:45	10:45 – 11:35	11:35 – 12:25	12:25 – 1:15
Mon			DEC		
Tue			DEC		
Wed	DEC Lab				
Thu				DEC Lab	
Fri			DEC		
Sat	DEC				

Year/ Session : 2023 (winter)	Semester from Date: 01/08/2023 To Date : 30/11/2023
Semester & Branch	3rd sem & E&TC
Subject with Code	Digital Electronics & Th.3
Name of the Faculty Member	Pinaki Bisoyi
No of Weeks:	No of Days per Week Class Allotted : 4

B.I.E.T., COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
			Unit-1 Basics OF Digital Electronics
A	1st	1/8/23	1.1 Number system - Binary, octal,
U		4/8/23	Decimal, Hexadecimal, - Conversion
G		5/8/23	from one system to another system.
U	2nd	7/8/23	1.2 Arithmetic operation Addition,
S		8/8/23	Subtraction, Multiplication,
T			division, 1's & 2's complement of binarys & subtraction using complements method.
		11/8/23	1.3 Digital codes & its application & distinguish between weighted & non-weighted code, Binary codes, excess-3 & gray codes.

Seen
Pradyumna
12.8.23

Signature of the Faculty: Updated 11/8/2023

Signature of the Principal/Course Co-ordinator/HOD: 11/8/23.

B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
	3rd	12/8/23 14/8/23	1.4 Logic Gates : AND, NOT, NOR, NAND, OR, Exclusive - OR, Exclusive NOR - Symbol, function, expression, truth table, & timing diagram.
		18/8/23 19/8/23	1.5 Universal gates & its realization. 1.6 Boolean algebra, Boolean expression, Demorgan's theorem
	4th	21/8/23 22/8/23 25/8/23	1.7 Represent logic expression, SOP & POS forms. 1.8 Karnaugh map (3 & 4 variable) & minimization of logical expressions, don't care condition

1/8/2023

Signature of the Faculty:

Signature of the Principal/Course Co-ordinator/HOD:

B.I.E.T., COURSE PLAN

ıth	Week	Class Day	Theory/Practical Topic
			Unit-2
			Combinational logic circuits
	5th	28/8/23	2.1 Halfadder, full adder, Half subtractor, full subtractor Serial & parrallel binary ubit adder.
S	1st	1/9/23	
E		2/9/23	
P	2nd	4/9/23	
T.			2.2 Multiplexer (4:1), De-multiplexer (1:4), Decoder, encoder, Digital comparactor (3 bit).
E		5/9/23	
M		8/9/23	
		9/9/23	
B	3rd	11/9/23	
E			2.3 Seven segment decoder. (Defination, relevance, gate level of circuit logic circuit, truth table, Applications of above)
R		12/9/23	
		15/9/23	

Signature of the Faculty: 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD: 1/8/23

B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
			2·4 Unit-3
			Sequential Logic Circuit
		16/09/23	3.1 Principle of flip-flops
	4th	18/9/23	operations, its types.
		22/9/23	3.2. SR flip-flop using
		23/9/23	NAND, NOR, Latch
	5th	25/9/23	(unclocked).
		26/9/23	3.3 Clocked SR, D, JK, T
OCTOBER		30/9/23	JK Master Slave flip-flop
	2nd	2/10/23	logic circuit, truth-table
			and applications.
		6/10/23	3.4 Concept of Racing & how
		7/10/23	it can be avoided.

Signature of the Faculty: upadhy 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD:

B.I.E.T., COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
			Unit-4
			Registers ; Memories & PLD
O	3rd	9/10/23	4.1 shift Registers - serial - in - serial out, serial - in - parallel out, parallel - in - serial - out, & parallel - in - parallel - out.
C		10/10/23	
T		13/10/23	
O			
B.			
E	4th	16/10/23	4.2 Universal shift registers. Applications.
R			
		17/10/23	4.3 Types of counters & Applications
	6th	20/10/23	4.4 Binary counter, Asynchronous ripple counter, (up & down) Decade counter, synchronous counter, Ring counter.

Signature of the Faculty: 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD: 1/8/23

B.I.E.T.,COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
NOVEMBER	1st	3/11/23	4.5 Concept of memories – RAM, ROM, Static RAM, Dynamic RAM, PS RAM.
		4/11/23	4.6 Basic concept of PLD & applications.

Signature of the Faculty: Updated 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD:

B.I.E.T., COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
			Unit-5 A/D and D/A Converters
N	2nd	6/11/23	5.1 Necessitity of A/D & D/A Converters.
O		7/11/23	5.2 D/A Conversion using R-2R or weighted resistor methods.
V		10/11/23	5.3 D/A Conversion using R-2R ladder (weighted resistors) n/ws.
E		11/11/23	5.4 A/D Conversion using Counter method.
M	3rd	13/11/23	5.5 A/D conversion using Successive approximate method.
B			
E			
R			

Signature of the Faculty 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD: 1/8/23

B.I.E.T., COURSE PLAN

Month	Week	Class Day	Theory/Practical Topic
			Unit-6
			Logic Families
N	3rd	14/11/23	6.1 Various logic families and categories according to the Ic fabrication process.
O		17/11/23	
V			
E			
M		18/11/23	6.2 Characteristics of digital Ics - propagation Delay, fan-out, fan-in, power dissipation, Noise Margin, power supply requirement, and speed with reference to logic families.
B	4th	20/11/23	
E		21/11/23	
R		24/11/23	

Signature of the Faculty: 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD:

B.I.E.T.,COURSE PLAN

th	Week	Class Day	Theory/Practical Topic
	5th	23/11/23 28/11/23	6.3 Features, circuit oper?, and various applications of TTL (NAND), CMOS (NAND & NOR).

Seen Imediyaw

ure of the Faculty: 1/8/2023

Signature of the Principal/Course Co-ordinator/HOD: 1/08/23