

3rd Sem ETC

BHARAT INSTITUTE OF ENGINEERING & TECHNOLOGY

SIVARAM VIHAR, GHATAKESWAR HILLS
MOHADA, BERHAMPUR (GM.)



STUDENT'S ATTENDANCE REGISTER

Time	9:05	9:55	10:45	11:35	12:25
Day	9:55	10:45	11:35	12:25	1:15
Mon			✓		
Tue	✓				
Fri					✓
Sat	✓				

Year/ Session

2nd year, 2021-22

Semester & Branch

3rd Sem & E&TC

Subject with Code

Digital Electronics & Th-3

Name of the Faculty Member

Manase Padhy

B.I.E.T.

SYLLABUS COVERAGE

TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.
<u>Unit-1</u>			
<u>Basics of Digital Electronics</u>			
1.1 Number System - Binary, octal, Decimal, Hexadecimal - Conversion from one system to another no. system.	16/9/22 19/9/22	Upadhyay	
1.2 Arithmetic operation - Addition, Subtraction, multiplication, Division, 1's & 2's complement of binary nos. & subtraction using complements method.	23/9/22 24/9/22	Upadhyay	Pradyumn 29/9/22
1.3 Digital codes & its application & distinguish bet ⁿ weighted & non-weighted code, Binary codes, excess-3 & Gray code.	25/9/22 28/9/22	Upadhyay	
1.4 Logic gates: AND, OR, NOT, NAND, NOR, Exclusive-OR	29/9/22	Upadhyay	Upadhyay 12/9/22

Seen
Pradyumn

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TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.
Exclusive-NOR - Symbol, function, expression, truth table & timing diagram.	30/9/22		
1.5 Universal gates & its Realisation	1/10/22	Upadhyay	
1.6 Boolean algebra, Boolean expression : SOP & POS Forms.	12/10/22	Upadhyay	
1.7 Represent logic Expression : SOP & POS Forms.	14/10/22	Upadhyay	Upadhyay 12/10/22
1.8 Karnaugh map - (3 & 4 variables) & minimization of logical expression don't care conditions.	15/10/22 17/10/22	Upadhyay	

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TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.				
<u>Unit-2</u>							
<u>Combinational Logic Circuits</u>							
2.1 Half adder, full adder, Half Subtractor, full subtractor Serial & parallel Binary 4bit adder.	18/10/22 21/10/22 22/10/22 23/10/22	M. Prabhakar	M. Prabhakar 12/9/22				
2.2 Multiplexer (4:1), De-multiplexer (1:4), Decoder, Encoder, Digital Comparator (3bit)	28/10/22 29/10/22 31/10/22			M. Prabhakar	M. Prabhakar 12/9/22		
2.3 Seven segment Decoder (Definition, relevance, gate level of circuit logic unit/circuit truth table, Applications of above).	1/11/22 4/11/22					M. Prabhakar	M. Prabhakar 12/9/22

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TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.
<u>Unit-3</u>			
<u>Sequential Logic Circuits</u>			
3.1 principle of flip-flops operation & its types.	5/11/22 7/11/22	Upadhyay	
3.2 SR flip-flop using NAND, NOR latch (unlocked)	11/11/22 12/11/22 14/11/22	Upadhyay	4.1
3.3 clocked SR, D, JK, T, JK Master slave flip-flops symbol, logic circuit, truth table, & application.	15/11/22 18/11/22 19/11/22 21/11/22	Upadhyay	4.2 4.3
3.4 Concept of Racing & how it can be avoided.	21/11/22	Upadhyay	4.4
			4.5

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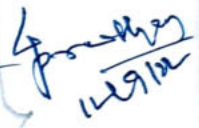


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TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.
<u>Unit-4</u>			
<u>Registers, Memories & PLD</u>			
4.1 Shift registers - serial-in-serial out, serial-in-parallel-out, parallel-in serial out & parallel-in-parallel-out	22/11/22 23/11/22 26/11/22	Upadhyay	Prakash 12/9/22
4.2 Universal shift registers Applications.	28/11/22	Upadhyay	
4.3 Types of counters & application	29/11/22	Upadhyay	
4.4 Binary counter, Asynchronous ripple counter (up & down)	2/12/22	Upadhyay	
Decade counter, synchronous Counter, Ring counter.	3/12/22		
4.5 Concept of memories - RAM, ROM, static RAM, dynamic RAM PS RAM	5/12/22 6/12/22	Upadhyay	Upadhyay 12/9/22

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TOPIC	DATE	SIGNATURE OF THE FACULTY	SIGNATURE OF THE H.O.D.
4.6 Basic concept of PLD & application.	9/12/22		
<p><u>Unit-5</u></p> <p><u>A/D & D/A Converters</u></p>			
5.1 Necessity of A/D & D/A Converters.	10/12/22		
5.2 D/A Conversion using weighted resistors method.	12/12/22		
5.3 D/A Conversion using R-2R ladders.			
5.4 A/D Conversion using Counter method.	13/12/22		
5.5 A/D Conversion using Successive approximate method.			

6.1

6.2

6.

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Unit-6

Logic FAMILIES

6.1 Various logic families & categories according to the IC fabrication process.

16/12/22

Upadhyay

6.2 Characteristics of digital ICs - propagation delay, fan-out, fan-in, power dissipation, noise margin, power supply requirement, & speed with reference to logic families.

17/12/22

20/12/22

Upadhyay

Prakash
12/12/22

6.3 Features, circuit operation, & various application of TTL (NAND), CMOS (NAND & NOR)

22/12/22

Upadhyay

Upadhyay
12/12/22

~~Prakash~~ Seen
18/12/22
Pradyumn
12.9.22